Introductory Ultra-Low-Voltage Electronics

C. Galup-Montoro, *Member, IEEE* , M. C. Schneider, *Member, IEEE,* L. G. de Carli, and M. B. Machado, *Student Member, IEEE*

***Abstract* — This paper presents the fundamentals for the design of MOS analog and digital circuits that can operate at very low supply voltages. Operation of the MOS transistor in the triode region is highlighted owing to the limited voltages available. Special attention has been given to the properties of the zero-VT transistor due to its high drive capability at low voltages. Ultra-low-voltage rectifiers using diodes or diode-connected MOSFETs operating in weak inversion are analyzed. The basic amplifiers and logic gates operating at ultra-low-voltage are then reviewed. Finally, simulation and measurement results for inductive-load oscillator prototypes built in 130 nm technology demonstrate that the oscillators can operate at supply voltages of the order of the thermal voltage *kT/q*.**

***Index Terms* —MOSFET ultra-low-voltage circuits, zero-VT transistors, ultra-low-voltage Colpitts oscillator, ultra-low-voltage rectifier circuits, energy harvesting**

I. Introduction

Continuous advancements in integrated circuit complexity and functionalities have allowed an impressive multiplication of all kinds of electronic devices for information processing, communications and consumer entertainment. According to the International Energy Agency (IEA), electronic devices currently account for 15 percent of household electricity consumption, and energy consumed by information and communication technologies as well as consumer electronics will double by 2022 and triple by 2030 [1]. Therefore, low-power electronics is not only mandatory for portable devices and future applications, like sensors for ambient intelligence and implantable bio-medical devices, but for all kinds of information processing devices. Voltage scaling is the most effective approach to enhancing energy efficiency [2].

If transistors could operate adequately at supply voltages as low as a few millivolts [3], the power consumed by the transistors could be reduced by a factor of one million, since the power consumption is proportional to the square of the voltage. Since technologies for millivolt switches are not yet available, we must exploit all the low voltage capabilities of CMOS technologies.

The progress toward low voltage operation has been slow. The first study on the CMOS inverter operating in weak inversion published in 1972 [4] revealed that CMOS logic circuits can operate at supply voltages as low as 200 mV at room temperature.

The use of feedback to match the subthreshold n- and p-channel MOSFET currents allowed digital CMOS circuits in a standard 180 nm CMOS technology to operate at V_{DD} =4kT/q [5] in 2001. More recently, operation at room temperature at V_{DD} = 62 mV was achieved using logic gates built around Schmitt triggers [6].

Concerning analog circuits, blocking oscillators using JFETs [7] or native MOSFETs [8] have attained impressive low supply voltage operation. The oscillators described in references [7] and [8] act as start-up circuits in off-the-shelf energy harvesting devices capable of operating from supply voltages as low as 20 mV, provided by thermoelectric generators. Reference [9] reports a blocking oscillator prototype circuit that starts to oscillate at a supply voltage of 5.5 mV at the expense of a bulky transformer.

We have designed rectifiers [10]-[14], and, more recently, oscillators [15]-[17] with supply voltages of the order of the thermal voltage kT/q, or even lower. It thus appears to us that there is no hard limit for the minimum supply voltage of analog circuits and we intend to exploit the potential of ultra-low-voltage (ULV) analog circuits to implement sensing devices with ultra-low-power consumption. These circuits will have a wide range of applications in passive devices that collect energy from the environment.

For circuits with supply voltages of 100 mV or less, transistors usually operate in weak inversion (WI). At these voltage levels, there is not enough voltage headroom to operate MOS transistors in saturation. For these reasons, in this study we used the model of the transistor operating in the triode region in WI, which is summarized in Section II.

The choice of an appropriate technology is of paramount importance for ULV circuits. MOS transistors with zero or near zero threshold voltage are particularly suitable for ULV circuits due to their current drive capability and sufficient voltage gain at very low supply voltages. Section III summarizes the characteristics of zero-VT MOSFETs.

For ULV design it is mandatory to use the correct physical parameters of the devices. For a diode, for example, the saturation current I_S is the appropriate physical parameter and not the threshold voltage, which is meaningless for ULV circuit design. In section IV we summarize the ultra-low-voltage operation of rectifiers implemented with diodes or diode-connected MOSFETs operating in weak inversion and the performance of an ULV rectifier designed in 130 nm CMOS technology.

In Section V we review the operation of the ideal common-source and common-gate amplifiers operating in the triode region and in weak inversion, which is the most appropriate inversion level for efficient ULV operation.

Section VI is dedicated to weak inversion CMOS logic.

ISBN 978-987-1907-44-1

IEEE Catalog Number: CFP1354E-CDR

In Section VII we show that analog circuits, such as oscillators built around zero-VT MOSFETs, can operate at supply voltages of the order of kT/q.

II. Ultra-Low-Voltage MOS Transistor Operation

Weak inversion (WI) (or close to weak inversion) is very attractive for ULV circuits since the transistor voltage gain is at its maximum for the available bias voltage.

In the triode region in weak inversion, the drift current is negligible, and the diffusion current is proportional to the carrier density gradient $(Q'_{IS}-Q'_{ID})/L$, where Q'_{IS} is the inversion charge density at the source, Q'_{ID} is the inversion charge density at the drain, and L is the channel length.

For an NMOS transistor the drain current is given [18] by

$$I_D = -W\mu\phi_t \frac{Q'_{IS}-Q'_{ID}}{L}, \qquad (1)$$

where W is the channel width, μ is the carrier mobility, ϕ_t is the thermal voltage and, interestingly, $\mu\phi_t$ is the diffusion coefficient.

In weak inversion the inversion charge density is an exponential function of the applied voltages [18], [19], as shown below:

$$Q'_{IS(D)} = Q'_{I0} e^{\left(\frac{V_G-V_T}{n\phi_t}-\frac{V_{S(D)}}{\phi_t}\right)}, \qquad (2)$$

where V_G, V_S, and V_D are the gate, source, and drain voltages referred to the bulk, respectively, $(V_G-V_T)/n$ can be regarded as the effective gate voltage in the channel, and n is called the slope factor and represents the capacitive divider of the oxide and depletion capacitances. The pre-exponential factor is independent of the applied voltages.

For an ideal MOs transistor (n =1) operating in WI, the carrier density as a function of the gate voltage given by Eq. (2) has an inverse logarithmic slope of 60 mV/ dec at 300K, as does the drain diffusion current given by Eq. (1).

We can calculate the source, drain and gate transconductances from (1) and (2) as

$$g_{ms} = -\frac{\partial I_D}{\partial V_S} = -\mu\frac{W}{L}Q'_{IS}, \qquad (3)$$

$$g_{md} = \frac{\partial I_D}{\partial V_D} = -\mu\frac{W}{L}Q'_{ID}, \qquad (4)$$

$$g_m = \frac{\partial I_D}{\partial V_G} = -\mu\frac{W}{L}\frac{Q'_{IS}-Q'_{ID}}{n} = \frac{g_{ms}-g_{md}}{n}. \qquad (5)$$

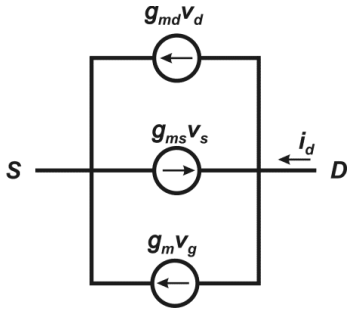

Fig. 1. Small-signal model of the MOSFET. Voltages are referenced to bulk.

Equation (5) represents the two essential features of the MOSFET operating in the triode region: a) The channel is represented by two anti-parallel current sources controlled by the source and drain voltages; and b) A gate voltage variation appears in the channel attenuated by n, which models the capacitive divider constituted by the oxide and depletion capacitances. The small-signal model of the MOSFET is shown in Fig. 1.

From (2), (3), and (4) it follows that

$$\frac{g_{ms}}{g_{md}} = e^{\frac{V_{DS}}{\phi_t}}. \qquad (6)$$

III. Technologies for ULV Circuits

In modern CMOS technologies, MOS transistors are usually available with several threshold voltages, as shown in Fig. 2. MOS transistors with zero or near zero threshold voltage are particularly suitable for ULV circuits due to their current drive capability at very low supply voltages, as is clear from Fig. 2. In MOSFETs, the inverse subthreshold (WI) slope (65 mV/dec and 78 mV/dec in Fig. 2) severely limits the operation of digital circuits at ultra-low voltage. In effect, at a supply voltage of 100 mV, the ratio of the on current to the off current (I_{ON}/I_{OFF}) is less than 50. The ideal ULV device would have a much lower inverse subthreshold slope allowing, for example, high I_{ON}/I_{OFF}, and high I_{ON} with only a couple of mV of power supply. It has been reported that tunnel FET (TFET) based on a band-to-band tunneling mechanism can obtain a steep inverse subthreshold slope of less than 60 mV/dec [20], but such technologies are not yet available for circuit fabrication. From the available technologies the zero-VT n-channel is the best device for ULV operation. However, zero-VT p-channel transistors are still not generally available.

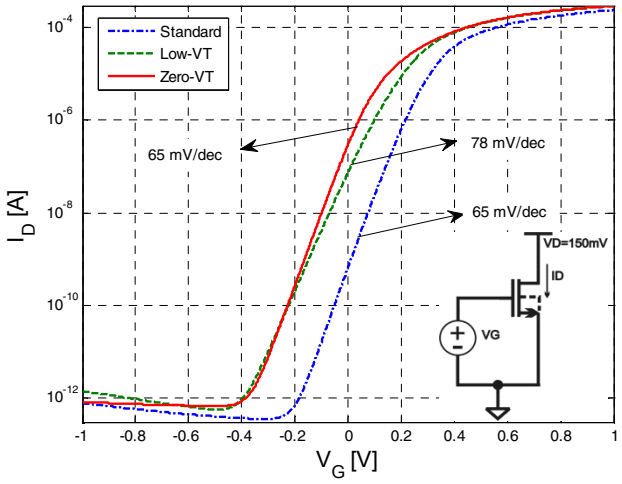

Fig. 2. I_D x V_{GS} (V_S=V_B) characteristics for standard, low and zero-VT n-channel transistors with W/L=3µm/0.42µm of a 130nm CMOS technology.

IV. Rectifiers and Voltage Multipliers at Ultra Low Voltage

Rectifiers are the basic building blocks of voltage multipliers, essential components for energy harvesting

circuits. The voltage levels available when harvesting energy from ambient sources can be very low, of the order of 100 mV, or even lower. The purpose of this section is to analyze the rectifier for input voltages which can be as low as the thermal voltage.

To simplify the mathematics, let us assume that the input signal for the rectifier of Fig. 3 is a symmetric square wave, with a 50% duty cycle. It is important to note that the results of the rectifier circuit for a sine wave input are similar to those obtained for a square wave input (for details, see [12], [13]).

We will also assume that the diode can be characterized through the Shockley (exponential) model, as given below

$$I_D = I_S[e^{\frac{qV_D}{nkT}} - 1]. \quad (7)$$

We will focus on the useful case in which the load capacitance is large enough to ensure a nearly constant output voltage. In this case, the steady-state operation of the circuit, for a peak input voltage greater than the thermal voltage, is illustrated in Fig. 3. As is clear from the figure, the diode forward current must be $2I_L+I_S$ in order to make the average diode current equal to the load current I_L. Thus, the voltage drop in the diode, according to (7), is

$$V_{on} = n\frac{kT}{q}\ln\left(1+\frac{I_P}{I_S}\right) = n\frac{kT}{q}\ln\left(1+\frac{2I_L+I_S}{I_S}\right). \quad (8)$$

Consequently, the output voltage of the rectifier is

$$V_0 \cong V_P - n\frac{kT}{q}\ln\left[2\left(1+I_L/I_S\right)\right] \quad (9)$$

In some electronic circuits, I_S can be as low as 1 fA and I_L as large as 1 mA. Assuming that n=1, we obtain, in this case

$$V_{on} = 26\cdot\ln\left(2\cdot10^{12}\right) \cong 796 \text{ mV}, \quad (10)$$

which is a typical voltage drop for a silicon diode. On the other hand, in a low-power/low-voltage application we can have, *e.g.*, I_S=I_L=1 μA. For n=1 we obtain

$$V_{on} = 26\cdot\ln\left(4\right) = 36 \text{ mV}. \quad (11)$$

Thus, the voltage drop in a forward-biased diode can be of the order of the thermal voltage, which is appropriate for low voltage and low power circuits. On the other hand, the low direct voltage drop leads to a reduction in the power efficiency of the converter, since the reverse current approximately equals the load current. Thus, the design of ultra-low-voltage rectifiers must provide a careful trade-off between the reverse diode currents and direct voltage drops, as we will see next.

In general, voltage multipliers are a cascade of elementary stages, such as that shown in Fig. 4.

The power conversion efficiency (PCE) of the voltage doubler is the output power divided by the input power. The latter is the sum of the output power and the power loss due to diodes D1 and D2 in Fig. 4.

An approximate expression of the PCE is [12]

$$PCE = \frac{P_{out}}{P_{out}+P_{loss}} \cong \frac{1-\frac{n\phi_t}{V_P}\ln\left[2\left(1+I_L/I_S\right)\right]}{\left(1+I_S/I_L\right)}. \quad (12)$$

The meaning of expression (12) is readily understood; the subtrahend in the numerator represents the power losses in the diodes during forward conduction while the addend in the denominator represents the power losses due to the reverse currents in the diodes. For a fixed input voltage, the PCE reaches its maximum for a given value of the ratio of the load current to the saturation current, *e.g.* I_L/I_S≅4 for $V_P/n\phi_t$ = 6, as shown in Fig. 5. This maximum is essential for the design of an efficient voltage multiplier. In fact, it has been shown in [12] that, for an N-stage multiplier, the maximum PCE is achieved when $V_L/Nn\phi_t$=I_L/I_S.

Note that in Fig. 5 the dc output voltage and the load current are both normalized to the diode parameters, namely $n\phi_t$ and I_S, respectively, thus providing important information concerning the design of integrated diodes for the required dc voltage and load current.

In integrated circuits the diodes are usually implemented using MOS transistors as shown in Fig.6.

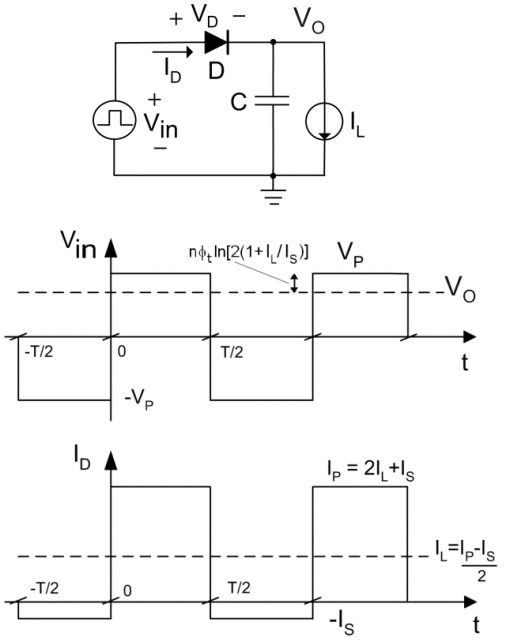

Fig. 3. Half-wave rectifier and voltage and current waveforms (after [16]).

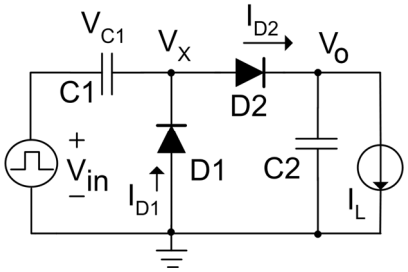

Fig. 4. Schematic of the voltage doubler analyzed herein.

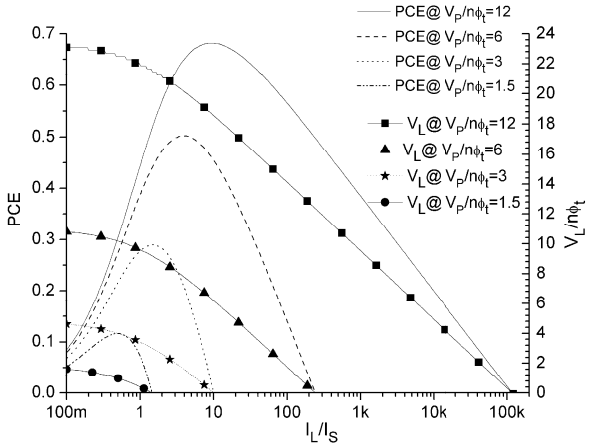

Fig. 5. Power conversion efficiency and load voltage of the voltage doubler versus normalized load current for $V_P/n\phi_t$ values of 1.5, 3, 6, and 12 (after [12]).

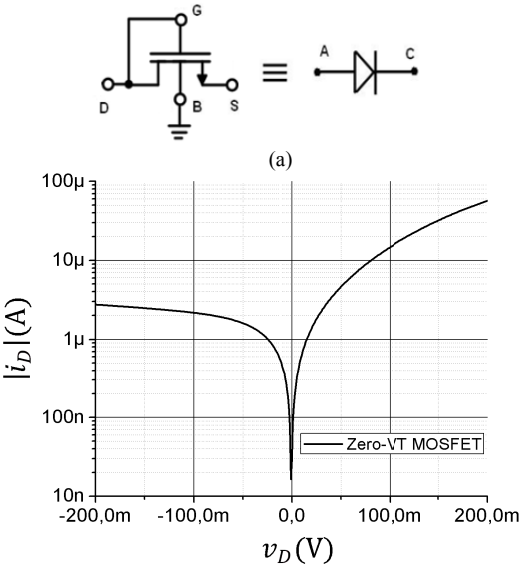

Fig. 6. (a) Diode connected MOSFET (b) low-voltage I-V characteristic of a diode-connected zero-VT transistor.

The layout of an integrated ac/dc converter including an LC-matching network designed to operate at 900 MHz is shown in Fig. 7. The voltage multiplier is comprised of 24 diode connected zero-VT transistors, a 38 nH (Q≈10) inductor, and a 100 fF compensation capacitor. Experimental results for the output voltage versus frequency are shown in Fig. 8. Note that the output voltage is relatively constant for a bandwidth of 100 kHz.

V. Basic Amplifiers

Using the model of section II for the MOSFET operating in WI in the triode region, the voltage gains of the common-gate and common-source topologies shown in Fig. 9 are, respectively,

$$A_{v,cg} = \frac{v_o}{v_i} = \frac{g_{ms}}{g_{md}} = e^{\frac{qV_{DS}}{kT}}, \text{ and} \qquad (13)$$

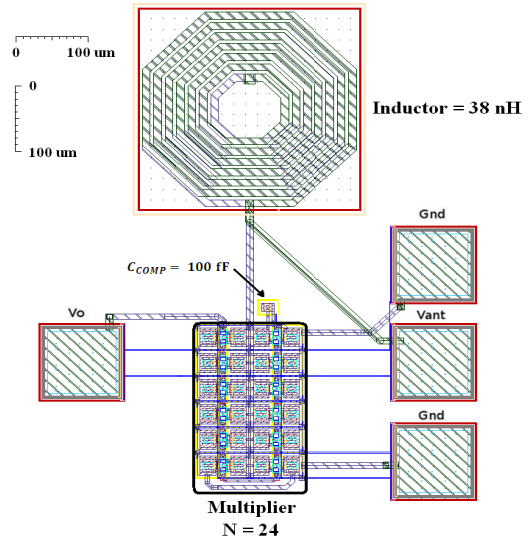

Fig. 7. Layout of the ac/dc converter fabricated in 130 nm CMOS technology.

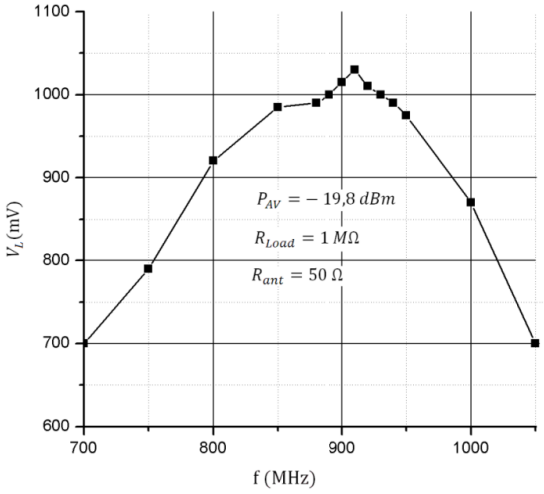

Fig. 8. Measured output voltage vs. frequency for the ac/dc converter whose layout is shown in Fig. 7 (the load resistance is 1 MΩ).

$$A_{v,cs} = \left|\frac{v_o}{v_i}\right| = \frac{g_m}{g_{md}} = \frac{g_{ms} - g_{md}}{ng_{md}} = \frac{1}{n}\left(e^{\frac{qV_{DS}}{kT}} - 1\right). \qquad (14)$$

Inverting (14) we determine V_{DS} as a function of the voltage gain, as

$$V_{DS} = (kT/q)\cdot\ln(1+nA_{v,cs}). \qquad (15)$$

For the common-source amplifier, the voltage gain equals unity for

$$V_{DS} = (kT/q)\cdot\ln(1+n). \qquad (16)$$

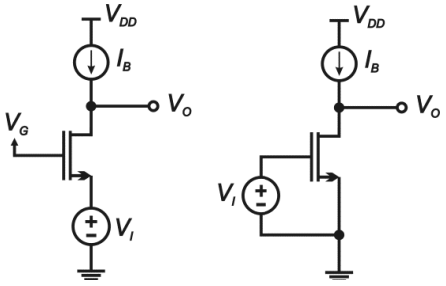

Fig. 9. The ideal common-gate and common-source amplifiers (I_B is an ideal current source).

On the other hand, the common-gate amplifier provides a voltage gain of greater than unity for $V_{DS}>0$. As will be seen later in this paper, this property of the common-gate amplifier is very useful for lowering the supply voltage limit for the operation of oscillators.

VI. LOGIC GATES

Regenerative logic circuits require a voltage gain larger than unity for their proper operation. The minimum supply voltage of regenerative CMOS logic can be found from the analysis of the static transfer curve of the inverter shown in Fig. 10(a). Considering, for simplicity, matched n- and p-channel MOSFETs, the maximum voltage gain occurs at the midpoint of the voltage transfer curve, as shown in Fig. 10(b). The V_{DS} voltage required to achieve unity gain is given by (16). Therefore, in the case of the "symmetric" CMOS inverter, the minimum supply voltage is $V_{DD}=2\cdot(kT/q)\cdot\ln(1+n)$ [21]. For ideal MOSFETs (*i.e.,* with zero depletion capacitance, $n = 1$) $V_{DDmin} = 36$ mV at room temperature. This value is called the Meindl low voltage limit for CMOS logic.

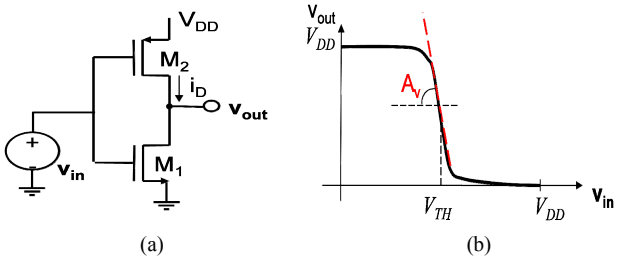

Fig. 10. (a) CMOS inverter, (b) voltage transfer characteristic.

Figure 11, taken from the pioneering work of Swanson and Meindl [4], clearly shows the effect of a supply voltage reduction on the transfer characteristic of a "symmetric" CMOS inverter. The logic threshold occurs at half the supply voltage. For supply voltages below 0.2 V, the reduction in the maximum voltage gain is clearly visible.

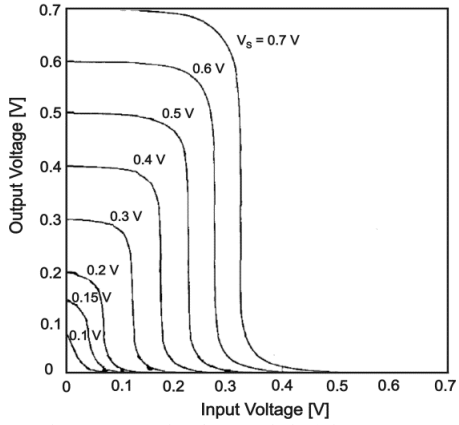

Fig. 11. CMOS inverter transfer characteristic (after [4]).

VII. OSCILLATORS

Since the oscillation condition requires a loop gain of unity, the minimum supply voltage expressions for oscillation are similar to expression (16). We begin by analyzing ring oscillators, which are common source topologies, as are the logic inverters. We then analyze a common-gate Colpitts oscillator. It is important to note that in the case of the common-gate topology, in contrast to the common source topology, there is no need for a minimum supply voltage to achieve unity gain. Furthermore, as we will see below, the minimum theoretical supply voltage to obtain oscillation in a Colpitts oscillator can be below kT/q.

A. The inductive-load ring oscillator

Starting up a conventional ring oscillator with a power supply below 100 mV is extremely difficult [22]. The magnitude of the minimum supply voltage V_{DD}(min) is usually limited by the imbalance of the threshold voltages of the n- and p-channel transistors of the logic inverter [22]. In order to reduce the V_{DD}(min) of the conventional ring oscillator, one can use the inductive-load ring oscillator topology [23] shown in Fig. 12. This topology, which replaces the active load PMOS of the logic inverter with an inductor, not only reduces V_{DD}(min) but also boosts the oscillation amplitude beyond the supply rail. It should be noted that for $N = 2$ this structure reduces to the widely-used cross-coupled LC oscillator.

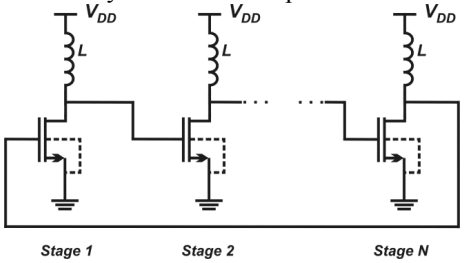

Fig. 12. Schematic diagram of an N-stage inductive-load ring oscillator.

Using the MOSFET model described in Section II, the simplified small-signal equivalent circuit of a single stage of the inductive-load ring oscillator is shown in Fig. 13, where g_m and g_{md} represent the gate and drain transconductances respectively, C is the sum of all capacitances between the drain node and the ac ground, and G_P models the inductor loss. The effect of C_{gd}, which is relevant due to both the overlap capacitance and operation of transistors in the triode region [17], has not been taken into account for the sake of simplicity.

The transfer function of the single stage in Fig. 13 is given by

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{md}+G_P}\frac{1}{1-j\tan\phi} \quad \text{and} \tag{17}$$

$$\tan\phi = \frac{1-LC\omega^2}{\omega L\left(g_{md}+G_p\right)}, \tag{18}$$

where ϕ is the phase shift between output and input.

The requirement of gain greater than unity for the starting up of oscillations is satisfied for

$$\frac{g_m}{g_{md}+G_P}\frac{1}{\sqrt{1+\left(\tan\phi\right)^2}} > 1 \cdot \tag{19}$$

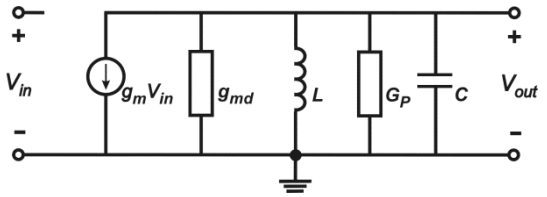

Fig. 13. Simplified small-signal model of a single stage of the inductive-load ring oscillator.

For the sake of simplicity, let us consider the case of an even number of stages. In this case, the ring oscillates with $\phi=\pi$. Thus, since $g_m = (g_{ms}-g_{md})/n$, (19) can be rewritten as

$$\frac{g_{ms}}{g_{md}} > 1 + n\left(1 + \frac{G_p}{g_{md}}\right). \qquad (20)$$

From (6) and (20), the minimum supply voltage required to start up the oscillator is

$$V_{DD}(\min) = V_{DS}(\min) = \phi_t \ln\left[1 + n\left(1 + \frac{G_p}{g_{md}}\right)\right]. \qquad (21)$$

If the inductor losses are negligible, (21) reduces to

$$V_{DD}(\min) > \phi_t \ln(1+n). \qquad (22)$$

Thus, the minimum supply voltage for oscillation is one-half of the minimum supply voltage required for proper operation of the logic inverter. This result was to be expected since, if the inductor is lossless, oscillation is achieved for an intrinsic gain of the transistor higher than unity, as required for one of the transistors of the CMOS inverter.

We designed a seven-stage inductive ring oscillator using zero-VT transistors. Since the phase shift at oscillation is dependent on the number of stages, this is also true for the minimum supply voltage for oscillation, as shown in Fig. 14. The micrograph of the circuit implemented in a 130 nm technology is shown in Fig. 15.

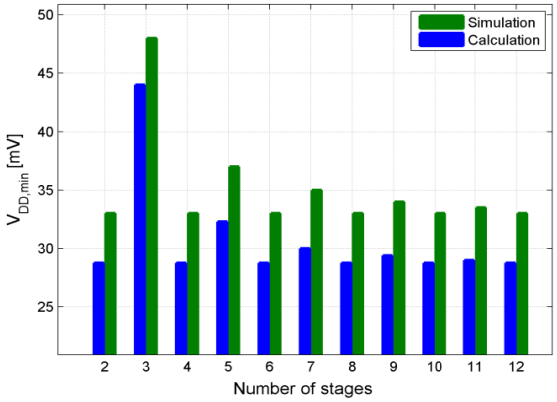

Fig. 14. Calculated and simulated $V_{DD,min}$ vs. number of stages N of the oscillator in Fig. 12 using a 130 nm technology (after [17]).

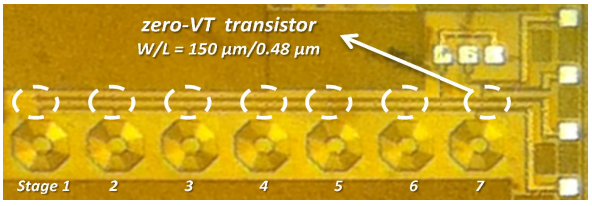

Fig. 15. Micrograph of the seven-stage inductive ring oscillator in 130 nm technology (after [17]).

A summary of the characteristics of the zero-VT transistor (W/L=150 µm/0.48 µm) and the inductor used in the oscillator is given in Table I. Note that G_P is much lower than g_{md} within the expected frequency range (500 to 800 MHz).

Table I.
Main characteristics of the inductor (@ 550 MHz) and transistor (V_{DD}=40 mV) used in the integrated inductive ring oscillator.

Transistor		Inductor
g_{md}* = 2.3 mA/V	C = 130 pF	L = 100 nH
V_T* = 22 mV	C_{gd} = 70 pF	G_P = 0.3 mA/V

* Experimental values.

Using the values shown in Table I, the calculated oscillation frequency is around 1 GHz, against 730 MHz obtained using the simulator. In fact, the parasitic capacitances introduced by a poor layout contributed to reducing the oscillation frequency to 550 MHz, as the experimental spectral diagram in Fig. 16 shows.

The minimum voltage required to start up the oscillator obtained with the experimental prototype was around 53 mV, very close to the calculated value of 50 mV.

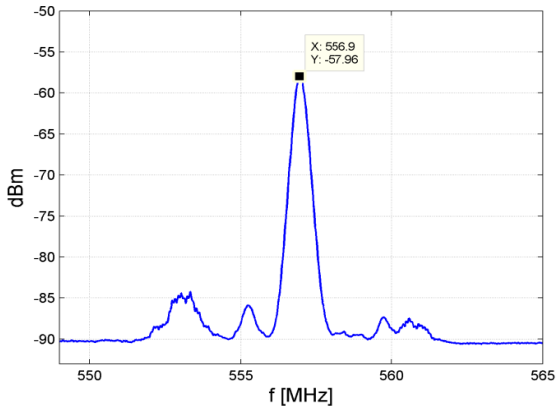

Fig. 16. Spectral diagram of the seven-stage inductive ring oscillator, obtained experimentally for V_{DD}=70 mV (after [17]).

B. The Enhanced Swing Colpitts Oscillator (ESCO)

In the conventional Colpitts oscillator [24] the supply voltage is divided between the active device and a DC current source (or resistor) connected to the active device. In order to apply all of the available bias voltage to the transistor we adopted the topology of Fig. 17, in which L_2 substitutes the DC current source of the conventional Colpitts oscillator [25]. This topology is called the enhanced-swing (ES) Colpitts oscillator because inductors L_1 and L_2 in series with the transistor channel allow the source/drain terminals to swing beyond the supply rails [25]. G_1 and G_2 model the losses of inductors L_1 and L_2, respectively.

The detailed analysis of the ES Colpitts is cumbersome [25] owing to the second tank composed of L_2 and C_2. In order to obtain some insight for circuit design we adopted the simplified approach of considering the capacitive feedback divider (C_1 and C2) as a transformer-like network with a turns

ratio of 1:C1/(C1+C2) [26]. The resulting simplified second-order resonator circuit is shown in Fig. 18.

As is clear from the equivalent circuit of Fig. 18, the oscillator start-up condition is achieved when the real part of the tank conductance is negative, which gives

$$g_{ms} > \left(1+\frac{C_2}{C_1}\right) g_{md} + \frac{C_1}{C_2} G_2 + \left(2+\frac{C_1}{C_2}+\frac{C_2}{C_1}\right) G_1 . \qquad (23)$$

The above expression is a generalization of the result presented in [15], since it explicitly includes the effect of the losses of L_2 on the start-up condition.

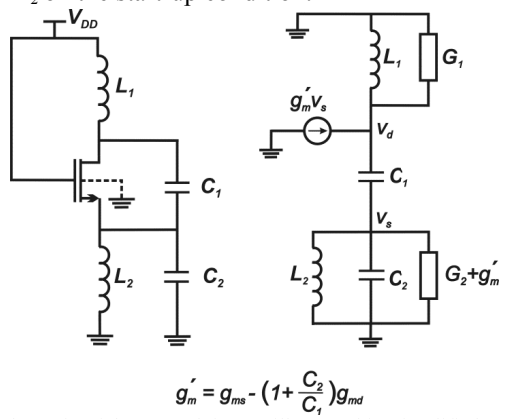

Fig. 17. Schematic of the ES Colpitts oscillator and its simplified small-signal model.

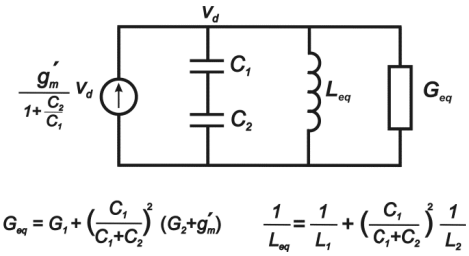

Fig. 18. Second-order small-signal model of the ES Colpitts oscillator.

The optimum value of the capacitor ratio which minimizes the transconductance necessary to start up oscillations, given by (23), is

$$\frac{C_2}{C_1} = \sqrt{\frac{G_1+G_2}{g_{md}+G_1}} . \qquad (24)$$

In the hypothetical case of ideal inductors and capacitors (G_1=G_2=0) it follows from (23) that

$$g_{ms} > \left(1+\frac{C_2}{C_1}\right) g_{md} . \qquad (25)$$

In this hypothetical case, for which the losses are only due to the transistor, the limit for the minimum supply voltage for oscillation start-up, which is obtained by combining (6) and (25), is

$$V_{DD\lim} = \frac{kT}{q} \ln\left(1+\frac{C_2}{C_1}\right) . \qquad (26)$$

For C_1=C_2, V_{DDlim} equals the voltage drop of a transistor at the Meindl limit [21], but for $C_2 < C_1$ the value of V_{DDlim} given by (26) is below it. Condition (26) would be observed for high-quality-factor passive devices, as is clear from (24).

Using the theoretical framework presented herein, we designed a Colpitts oscillator for operation at 800 MHz. At this frequency, the inductors have a quality factor of around 13. The oscillator was designed to operate with a wide zero-VT transistor with W/L=1500 µm/420nm. At 50 mV of voltage supply, its transistor gain (g_{ms}/g_{md}) is ≈ 2.2 and its drain transconductance is ≈ 25 mA/V. A schematic diagram of the oscillator, as well as the voltage buffer, is shown in Fig. 19. The buffer inverter chain topology was chosen to reduce the capacitive load of the oscillator. In Fig. 19 the inductor parameters (characterized at 800 MHz) and the MOSFET capacitances, extracted using the Spectre/Cadence simulator, are indicated. A micrograph of the circuit implemented in the IBM 130 nm technology is shown in Fig. 20.

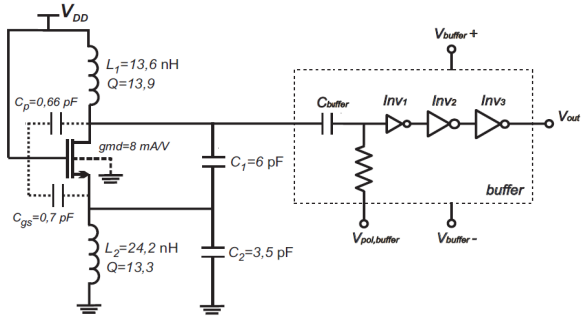

Fig. 19. Schematic diagram of the ESCO design for operation at 800 MHz and its voltage buffer. Inductors were characterized at 800 MHz through simulation.

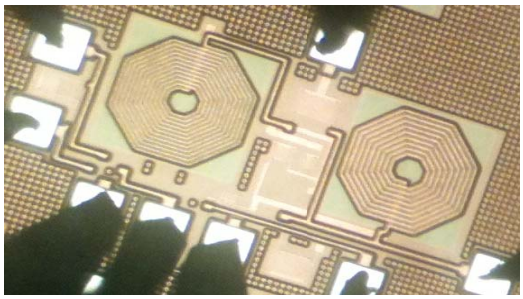

Fig. 20. Micrograph of the ESCO built in 130 nm technology.

The set-up used to test the oscillator is shown in Fig. 21. As can be seen in the figure, the circuit can oscillate below 100 mV of supply voltage, starting up from around 86 mV. Measurements with the experimental prototype show that the frequency of oscillation is around 700 MHz against 715 MHz obtained in a post-layout simulation. The ESCO spectral diagram is shown in Fig. 22 for V_{DD} = 86 mV.

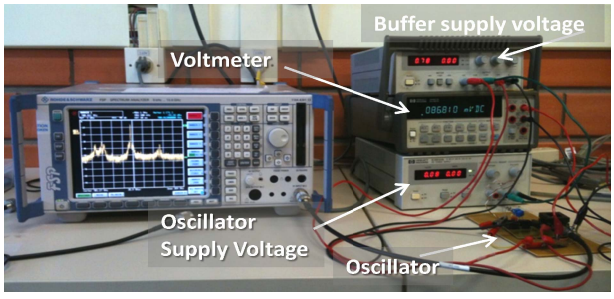

Fig. 21. Set-up used to test the ESCO.

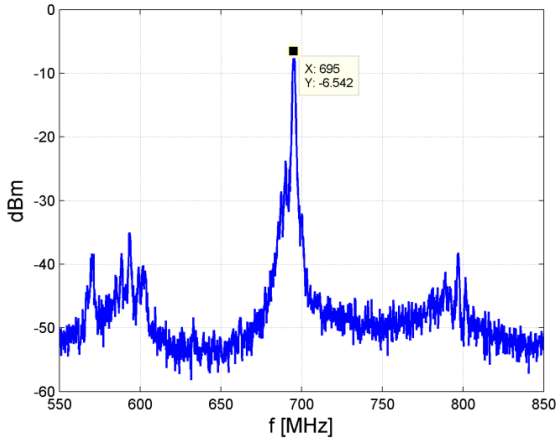

Fig. 22. Spectral diagram of the ESCO (V_{DD} = 86 mV).

The minimum V_{DD} for sustained oscillations of the ESCO presented is considerably higher than the value of 20 mV in reference [16], but it is worth noting that the Colpitts oscillator in [16] uses high-quality off-the-shelf components whereas the oscillator presented here is fully integrated.

VIII. CONCLUSIONS

We have briefly discussed rectifiers, amplifiers, logic gates and oscillators operating at ultra-low voltage using an exponential law for the non-linear device (diode or MOSFET). We found that the minimum supply voltage for the proper operation of the analog circuits can be below the Meindl limit for CMOS logic. We proposed the use of zero-VT MOSFET for the operation of ULV analog circuits. Moreover, we discussed the use of high-quality-factor passives and the enhanced-swing Colpitts topology for a ULV oscillator. Experimental results showed the operation of integrated voltage multipliers and oscillators with input (supply) voltages of the order of the thermal voltage.

ACKNOWLEDGMENTS

Acknowledgments are due to MOSIS for the fabrication of the devices and to the Brazilian Federal Government agencies CNPq and CAPES for the partial funding of this study.

REFERENCES

[1] M. Ellis, *Gadgets and Gigawatts, Policies for Energy Efficient Electronics.* Paris, FR: International Energy Agency IEA/OECD, 2009.
[2] M. Alioto, Guest editor, Special issue on ultra-low-voltage VLSI circuits and systems for green computing, *IEEE Trans. on Circuits and Syst. II, Exp. Briefs*, pp. 849-852, Dec. 2012.
[3] Center for Energy Efficient Electronics Science, available on line at https://www.e3s-center.org/.
[4] R. M. Swanson and J. D. Meindl, "Ion-implanted complementary MOS transistors in low voltage circuits," *IEEE J. Solid State Circuits*, vol. 7, pp. 146-153, Apr. 1972.
[5] A. Bryant et al. "Low-power CMOS at Vdd = 4kT/q," *Device Research Conference*, pp. 22-23, Notre Dame, IN, June 2001.
[6] N. Lotze, and Y. Manoli, "A 62 mV 0.13µm CMOS standard-cell-based design technique using Schmitt-trigger logic," *IEEE J. Solid-State Circuits*, vol. 47, no. 1 pp. 47-60, Jan. 2012.
[7] ECT310 datasheet, available on-line at http://www.enocean.com.
[8] LTC3108 datasheet, available on-line at http://www.linear.com.
[9] Oscillator with super low supply voltage, On-line available http://www.dicks-website.eu/fetosc/enindex.htm, accessed April 16, 2012.
[10] A. Jair Cardoso, M. C. Schneider, C. Galup-Montoro; "Design of very low voltage CMOS rectifier circuits"; *IEEE Circuits and Systems for Medical and Environmental Applications Workshop* (CASME 2010), Mérida, Mexico, Dec. 2010.
[11] A. J. Cardoso, M. C. Schneider, C. Galup-Montoro; "Teaching low voltage electronics: the case of the rectifier circuit," IEEE International Conference on Microelectronic Systems Education (MSE), San Diego, USA, 2011, pp.29-30, 5-6 June 2011.
[12] A. J. Cardoso, L. G. de Carli, C. Galup-Montoro, and M. C. Schneider, "Analysis of the rectifier circuit valid down to its low-voltage limit" , *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 106 - 112, Jan. 2012.
[13] A. J. Cardoso, "Modelagem e projeto de conversores AC/DC de ultrabaixa tensão de operação," PhD thesis, Federal University of Santa Catarina (UFSC), 2012.
[14] L. G. de Carli, "Modelagem e projeto de retificadores de múltiplos estágios para ultrabaixa tensão de operação," Engineering Degree Final Project, Federal University of Santa Catarina (UFSC), 2013.
[15] F. Rangel de Sousa, M. B. Machado, and C. Galup-Montoro, "A 20 mV Colpitts oscillator powered by a thermoelectric generator," in *Proc. IEEE Int. Symp. on Circ. and Systems*, pp. 2035-2038, Seoul, Korea, May 2012.
[16] C. Galup-Montoro, M. C. Schneider, and M. B. Machado, "Ultra-low-voltage operation of CMOS analog circuits: amplifiers, oscillators, and rectifiers," *IEEE Trans. on Circuits and Syst. II, Exp. Briefs*, vol. 59. no.12, pp. 932-36, Dec. 2012.
[17] M. B. Machado, M. C. Schneider, C. Galup-Montoro, "Analysis and design of ultra-low-voltage inductive ring oscillators for energy-harvesting applications," *IEEE Latin American Symp. on Circuits and Syst. (4th LASCAS)*, Cusco, Peru, Feb. 2013.
[18] M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*. Cambridge University Press, 2010.
[19] C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *J. of Analog Integrated Circuits and Signal Processing*, vol. 8, no. 7, pp. 83-114, July 1995.
[20] H.-Y. Chang et al., "Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing," *IEEE Trans. on Electron Devices*, vol. 60, no. 1, pp. 92-96, January 2013.
[21] J. D. Meindl and A. J. Davis, "The fundamental limit on binary switching energy for terascale integration (TSI)," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1515-1516, Oct. 2000.
[22] T. Niiyama et al., "Dependence of minimum operating voltage (VDDmin) on block size of 90-nm CMOS ring oscillators and its implications in low power DFM," *9th Int. Symp. on Quality Electronic Design*, pp.133-136, San Jose, Mar. 2008.
[23] J. Savoj and B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with a half-rate binary phase/frequency detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 13-21, Jan. 2003.
[24] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, Boston, 2001.
[25] T. W. Brown, F. Farhabakhshian, A. G. Roy, T. S. Fiez, and K. Mayaram, "A 475 mV, 4.9 GHz enhanced swing differential Colpitts VCO with phase noise of -136 dBc/Hz at a 3 MHz offset frequency," *IEEE J. Solid-State Circuits*, vol. 46, no. 8 pp. 1782-1795, Aug. 2011.
[26] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*, Addison-Wesley Publishing Company, Reading, MA, 1971.